## AMENDMENTS TO THE CLAIMS

1-27. (canceled)

28. (new) A method of determining a value of a resistance in a circuit comprising steps of:

cyclically discharging a capacitance through the resistance;

determining a duty cycle of a recharging signal for the capacitance; and

obtaining the value of the resistance from the duty cycle of the recharging signal.

29. (new) A method of determining a value of a resistance as in claim 28, wherein the recharging signal for the capacitance is a substantially constant current.

30. (new) A method of determining a value of a resistance as in claim 28, wherein the recharging signal is pulsed, and the duty cycle is determined by counting recharging signal pulses during a sensing period.

31. (new) A method of determining a value of a resistance as in claim 30, wherein the capacitor is charged prior to a start of the sensing period.

32. (new) A method of determining a value of a resistance as in claim 30, wherein the circuit includes a resistance-based memory.

33. (new) A method of determining a value of a resistance as in claim 32, wherein the resistance-based memory is an MRAM.

34. (new) A method of measuring the value of a resistance comprising:

producing a plurality of electrical pulses at a rate related to the resistance;

counting the electrical pulses over a predetermined time period to produce a pulse count; and

evaluating the pulse count to determine the resistance.

35. (new) A method according to claim 34 wherein each electrical pulse comprises a pulse of substantially uniform width.

36. (new) A method according to claim 34 wherein the evaluating comprises comparing the pulse count to a reference pulse count to determine the value of the resistance.

37. (new) A method according to claim 36 wherein the evaluating further comprises determining the resistance as one value if the pulse count is above the reference pulse count and as another value if the pulse count is below the reference pulse count.

38. (new) A method for sensing a value of a resistance comprising:

charging a capacitance to a voltage level;

discharging the capacitance through the resistance;

generating at least one recharging pulse each time the voltage on the capacitor falls below a predetermined value;

using the recharging pulse to recharge the voltage on the capacitor; and

determining the resistance from the number of recharging pulses which are generated during a predetermined period of time.

39. (new) A method as defined in claim 38 wherein the discharging includes discharging the capacitor through the resistor at a substantially constant current.

40. (new) A method of measuring a resistance of a resistor comprising:

applying a known voltage across the resistor such that a first current flows through the resistor;

withdrawing a current equal to the first current from a capacitor having a charge thereon;

replenishing the charge on the capacitor with a plurality of current pulses, such that one pulse of the plurality is applied to the capacitor when a voltage measured across the capacitor falls below a threshold voltage;

counting the plurality of pulses over a finite time period; and

determining a resistance of the resistor based on the counted pulses.

41. (new) A method as in claim 40 further comprising comparing a value of counted pulses to a predetermined value to determine the resistance.

42. (new) A method as in claim 41 wherein when a value of counted pulses is above a reference value, the resistance is determined as having one value and when a value of counted pulses is below the reference value the resistor is determined as having another value.

43. (new) A method of measuring an impedance comprising:

applying a substantially uniform voltage across the impedance;

flowing a substantially uniform current into the impedance from a charge reservoir;

flowing a plurality of current pulses into the charge reservoir;

controlling the flow of the plurality of current pulses in response to a quantity of charge in the charge reservoir;

counting the plurality of current pulses over a definite time to produce a pulse count; and

relating an impedance value to the pulse count.

44. (new) A method as defined in claim 43 wherein the impedance is an electrical resistance.

45. (new) A method as defined in claim 43 wherein the impedance is a capacitance.

46. (new) A method as defined in claim 43 wherein the impedance is an inductance.

47. (new) A method for making a memory integrated circuit comprising steps of:

assembling a first circuit for conducting current from a capacitor through a resistor, the first circuit including a controlled current source for delivering current to the capacitor;

providing a comparator for comparing a voltage on the capacitor to a reference voltage and supplying a pulse to turn on the current source when the voltage on the capacitor falls below the reference voltage;

operatively connecting a pulse counter to the comparator output for counting pulses generated by the comparator; and

providing a second circuit for determining the value of the resistance based on a count value stored in the pulse counter.

48. (new) A method for making a memory integrated circuit as defined in claim 47, further comprising providing a clock input to the comparator, and arranging the comparator such that the output of the comparator changing state only when a clock signal applied to the clock input changes state.

49. (new) A method for making a memory integrated circuit as defined in claim 47, further comprising arranging the second circuit to compare the value stored in the pulse counter to a reference value and determine whether the stored value is greater or less than the reference value.

50. (new) A method for making a memory integrated circuit as defined in claim 49, further comprising steps of:

assembling the first circuit to include a transistor having a source operatively connected to the capacitor, a gate, and a drain; and

operatively connecting a differential amplifier having a non-inverting input connected to a first reference voltage, an output operatively connected to the gate, and an inverting input operatively connected to the drain and to the resistor.

51. (new) A method for making a memory integrated circuit as defined in claim 50, further comprising including in the second circuit a digital comparator adapted to receive the value stored in the pulse counter, receive a reference value, and compare the stored value to the reference value to produce an output.

52. (new) A device state sensing circuit comprising:

a controlled voltage supply;

an electronic charge reservoir;

a current source; and

a pulse counter;

wherein the controlled voltage supply is operatively connected to an element of a memory device to maintain a substantially constant voltage across a resistive element;

the electronic charge reservoir is operatively connected to the controlled voltage supply to provide a current through the resistive element;

the current source is operatively connected to the charge reservoir to repeatedly supply a pulse of current to recharge the charge reservoir upon a predetermined depletion of electronic charge from the reservoir; and

the pulse counter count is a number of the pulses supplied by the current source over a predetermined time period, the contents of the pulse counter representing a logic state of the memory cell.